WHAT IS CLAIMED IS:

1. A computer system comprising:

an integrated core and graphic controller device including a core logic controller portion and a graphic controller portion;

a system memory pool;

a stand-alone frame buffer memory pool separate from said system memory pool;

a first memory data bus interconnecting said integrated core and graphic controller device and said system memory pool;

a second memory data bus interconnecting said integrated core and graphic controller device and said frame buffer memory pool; and

a memory address and control signal bus interconnecting said integrated core and graphic controller device, said system memory pool and said frame buffer memory pool;

said graphic controller portion of said integrated core and graphic controller device being capable of generating a same set of address signals received by said system memory pool and said frame buffer memory pool via said memory address and control signal bus such that said graphic controller portion is able to access simultaneously first word part display data from said system memory pool via said first memory data bus and second word part display data from said frame buffer

memory pool via said second memory data bus.

2. The computer system as claimed in Claim 1, wherein each of the first and second word part display data is a quad-word part data.

3. The computer system as claimed in Claim 2, wherein the first and second word part display data simultaneously accessed by said graphic controller portion from said system memory pool and said frame buffer memory pool form bi-quad-word display data.

4. The computer system as claimed in Claim 3, wherein each of the first and second word part display data includes 64 data bits.

5. The computer system as claimed in Claim 3, wherein the first word part display data is low word part display data, and the second word part data is high word part display data.

6. The computer system as claimed in Claim 1, wherein said system memory pool is formed from standard DIMM, and said frame buffer memory pool is formed from discrete memory chips.